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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,110	DE SANTIS ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *29 and 32-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28,30 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/15/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-40 are presented for examination in this application (10,722,110) filed on November 25, 2003.

Acknowledge is made of information disclosure document filed on 3/15/2004.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-31, drawn to structure and operations of a flash memory device controller, classified in class 711, subclass 103.

II. Claims 32-37, drawn to application specific algorithms, classified in class 700, subclass 89.

III. Claims 38-40, drawn to plural processor systems, classified in class 700, subclass 2.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as apparatus and application for its practice. The inventions are distinct if it can be shown that either: (1) the application as claimed can be practiced by another and materially different apparatus, or (2) the apparatus as claimed can be used to practice another and materially different application. (MPEP § 806.05(e)). In this case the apparatus, i.e., the structure and operations of a flash memory device controller, as claimed can be used in a materially different application while a materially different apparatus can be used to execute the algorithms of the specific application as claimed.

Inventions I and III are related as apparatus and system for its practice. The inventions are distinct if it can be shown that either: (1) the system as claimed can be constructed by another and materially different apparatus, or (2) the apparatus as claimed can be used to practice another and materially different system. (MPEP § 806.05(e)). In this case the apparatus, i.e., the structure and operations of a flash memory device controller, as claimed can be used in a materially different system with singular or multiple processors, while the dual processor system as claimed can have a materially different apparatus.

Inventions II and III are related as application and system for its practice. The inventions are distinct if it can be shown that either: (1) the system as claimed can be used to practice another and materially different application, or (2) the application as claimed can be used to practice another and materially different system. (MPEP § 806.05(e)). In this case the application, i.e., data pattern checking, as claimed can be used in a materially different system with singular or multiple processors, while the dual processor system as claimed can have a materially different application.

Because these inventions are independent or distinct for the reasons given above and have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

3. During a telephone conversation with Mr. Tod A. Myrum (Reg. No. 42,922) on April 24, 2006 a provisional election was made without traverse to prosecute the invention of structure and operations of a flash memory device controller, claims 1-31. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 32-40 have been withdrawn from further consideration by the examiner, per 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Objections

4. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Claim 29 is missing is this Application. In order to preserve the numbering of the claims as they are currently presented, claim 29 is treated as a cancelled claim for the purpose of claim analysis in this Office Action.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 6-8, 11, 13-15, 17-20 and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Robinson (U.S. 5,937,423).

As to claim 1, Robinson discloses **a memory device controller** [figure 3 shows a flash memory device (27) and the associated controller (the interface, 30)] **comprising**:

an updateable register bank [a group of registers (figure 3, 32~58) comprising command register (32), status register (33), source address register (34), destination address register (35), length register (36), erase queue register (37), data I/O register (38) and data I/O register (58); all these registers are programmable (i.e., updateable)

by the CPU (figure 1, 11) via the CPU/PCI Bus/Memory bridge (figure 1, 14) and the local bus (figure 1, 12)] **adapted to send a first signal** [the corresponding first signal is the address signal (address decoder, figure 3, 63)] **to an analog/memory core of the memory device** [blocks of flash EEPROM memory cells (figure 3, 68)] **for controlling operation of the analog/memory core** [column 8, lines 24-60], **the analog/memory core comprising an array of flash memory cells** [blocks of flash EEPROM memory cells (figure 3, 68)] **and supporting analog access circuitry** [For the embodiment illustrated, a first byte defines the minimum power supply voltage used with the array in its normal operating condition. A second byte defines the maximum power supply voltage used with the array in its normal operating condition. A third byte defines the minimum power supply voltage used with the array in its programming condition. A fourth byte defines the maximum power supply voltage used with the array in programming condition. The next eight bytes define various system timing parameters for different operations (column 11, lines 10-20); high voltage, figure 3, 61]; **a bus controller** [the CPU/PCI Bus/Memory bridge (figure 1, 14)] **coupled to the register bank** [via the local bus (figure 1, 12); figure 3], **the bus controller adapted to receive a second signal** [the corresponding second signal may be one of the output data (data multiplexer, figure 3, 62)] **from the register bank** [via the local bus (figure 1, 12); figure 3] **and to send a third signal** [the third signal may be the command (command register, figure 3, 32)] **to the register bank for updating the register bank** [via the local bus (figure 1, 12); figure 3, "data and command in"];

a select register [register select, figure 3, 59] **coupled to the register bank** [as shown in figure 3]; **and**

a first processor [the CPU, figure 1, 11] **coupled to the bus controller and the select register** [all these registers are programmable (i.e., updateable) by the CPU (figure 1, 11) via the CPU/PCI Bus/Memory bridge (figure 1, 14) and the local bus (figure 1, 12); figure 3].

As to claim 2, Robinson teaches that **the memory device controller of claim 1, further comprising an expression checker coupled between the first processor and the bus controller** [the expressions to be checked are stored in the query mode ROM (figure 3, 31) and the data may be read on the bus (figure 1, 12) by the processor (figure 1, 11) to determine the details of the flash memory and the type of operations that may be performed (column 9, lines 15-45); FIG. 4 also illustrates a second twelve bytes that provide a description (i.e., expression) of the system interface and are returned in response to a query command (column 10, lines 25-28)].

As to claim 3, Robinson teaches that **the memory device controller of claim 1, further comprising a transfer register** [the corresponding transfer register is the command register (figure 3, 32)] **coupled to the bus controller** [as shown in figures 1 and 3] **for receiving the third signal** [the third signal is the command (command register, figure 3, 32)] **therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase** [The data returned may be sent to the register 38 and be clocked serially in a

preordered sequence so that it may be read on the bus 12 by a processor (column 9, lines 20-23)].

As to claim 4, Robinson teaches that **the memory device controller of claim 1, further comprising a clock for sending clock signals to at least one of the first processor, the register bank, and the select register** [The data returned may be sent to the register 38 and be clocked serially in a preordered sequence so that it may be read on the bus 12 by a processor (column 9, lines 20-23)].

As to claim 6, Robinson teaches that **the memory device controller of claim 1, further comprising a controller interface coupled to the first processor** [all these registers are programmable (i.e., updateable) by the CPU (figure 1, 11) via the CPU/PCI Bus/Memory bridge (figure 1, 14) and the local bus (figure 1, 12)] **and couplable to at least one of a command user interface** [each flash EEPROM device of the array includes a command user interface (CUI) including one or more state machines (column 7, lines 31-33); the command user interface within each of the flash memory devices are typically used for erasing the blocks of cells and reading or writing data ... (column 7, lines 41-47)] **of the memory device** [the local bus (figure 1, 12)] **and a second processor located externally of the memory device** [a second processor may be the local bus master shown in figure 1].

As to claim 7, Robinson teaches that **the memory device controller of claim 6, wherein the controller interface comprises a suspension controller for causing a suspend command received thereat to be sent to the first processor at a pre-selected time of an operating cycle of the memory device controller** [whether

functions such as erase and write may be suspended, the reasons for which suspendable functions may be suspended (column 9, lines 39-41)].

As to claim 8, Robinson teaches that **the first signal comprises an address of the analog/memory core** [the corresponding first signal is the address signal (address decoder, figure 3, 63)].

As to claim 11, Robinson discloses **a memory device controller comprising: an updateable register bank adapted to send a first signal to an analog/memory core of the memory device for controlling operation of the analog/memory core** [refer to "As to claim 1"];

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank; a select register coupled to the register bank [refer to "As to claim 1"];

a first processor coupled to the bus controller and the select register [refer to "As to claim 1"];

an expression checker coupled between the first processor and the bus controller [refer to "As to claim 2"];

a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase [refer to "As to claim 3"]; **and**

a controller interface coupled to the first processor and couplable to at least one of a command user interface [refer to "As to claim 6"] **of the memory device and a second processor located externally of the memory device** [refer to "As to claim 6"].

As to claim 13, refer to "As to claim 7" presented earlier in this Office Action.

As to claim 14, Robinson discloses **a memory device comprising**

an analog/memory core comprising an array of flash memory cells and supporting analog access circuitry [blocks of flash EEPROM memory cells (figure 3, 68)];

a memory device controller comprising:

an updateable register bank adapted to send a first signal to the analog/memory core for controlling operation of the analog/memory core [refer to "As to claim 1"];

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank [refer to "As to claim 1"];

a select register coupled to the register bank [refer to "As to claim 1"]; **and**

a first processor coupled to the bus controller and the select register [refer to "As to claim 1"]; **and**

a command user interface coupled to the first controller and couplable to a second processor located externally of the memory device [refer to "As to claim 6"].

As to claim 15, refer to "As to claim 2" presented earlier in this Office Action.

As to claim 17, refer to "As to claim 7" presented earlier in this Office Action.

As to claim 18, Robinson discloses **a memory device comprising an analog/memory core comprising an array of flash memory cells and supporting analog access circuitry** [blocks of flash EEPROM memory cells (figure 3, 68)];

a memory device controller comprising:

an updateable register bank adapted to send a first signal to the analog/memory core for controlling operation of the analog/memory core [refer to "As to claim 1"];

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank [refer to "As to claim 1"];

a select register coupled to the register bank [refer to "As to claim 1"]; **and**

a first processor coupled to the bus controller and the select register [refer to "As to claim 1"];

an expression checker coupled between the first processor and the bus controller [refer to "As to claim 2"];

a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase [refer to "As to claim 3"]; **and**

a command user interface coupled to the first controller and couplable to a second processor located externally of the memory device [refer to "As to claim 6"].

As to claim 19, refer to "As to claim 18" presented earlier in this Office Action.

As to claim 20, refer to "As to claim 2" presented earlier in this Office Action.

As to claim 22, refer to "As to claim 7" presented earlier in this Office Action.

As to claim 23, refer to "As to claim 3" presented earlier in this Office Action.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,937,423).

As to claim 5, Robinson does not mention that **the clock comprises four clock phases.**

However, Robinson teaches that the data returned may be sent to the register 38 and be clocked serially in a preordered sequence so that it may be read on the bus 12 by a processor (column 9, lines 20-23), which implies that a series of clocks are used to facilitate the operations. The exact number of clocks, be it three, four or five, may vary depending each operations and lacks patentable significance.

Claim Rejections - 35 USC § 102

8. Claims 1-4, 6, 8-12, 14-16, 18-28 and 30-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Sukegawa et al. (U.S. 5,603,001).

As to claim 1, Sukegawa et al. disclose **a memory device controller** [figure 2, 12] **comprising**:

an updateable register bank [figure 2 shows a group of programmable registers is associated with external bus interface (figure 2, 17) comprising registers 171~178] **adapted to send a first signal** [the corresponding first signal is the address signal (address conversion table, figure 2, 132)] **to an analog/memory core of the memory device** [blocks of NAND EEPROM memory cells (figure 2, 11-1~11-16)] **for controlling operation of the analog/memory core** [column 14, lines 16-65; column 15, lines 1-20], **the analog/memory core comprising an array of flash memory cells** [blocks of NAND EEPROM memory cells (figure 2, 11-1~11-16)] **and supporting analog access circuitry** [figure 2];

a bus controller [the corresponding bus controller comprises the MPU bus interface unit (figure 2, 15a) and the NAND bus interface (figure 2, 19)] **coupled to the register bank** [the MPU bus interface unit (figure 2, 15a) and the NAND bus interface (figure 2, 19) are coupled to the external bus interface (figure 2, 17) as shown in figure 2], **the bus controller adapted to receive a second signal** [the corresponding second signal may be one of the command (command register, figure 2, 176), for example, a command to inquire about the status of the NAND EEPROM] **from the register bank** [external bus interface (figure 2, 17) comprising registers 171~178] **and to send a third signal** [the third signal may be the status of the NAND EEPROM when the

command is to inquire about the status of the NAND EEPROM] **to the register bank for updating the register bank** [to update the status of the NAND EEPROM];

a select register [the address conversion table, figure 2, 132, contains the address information of an entity to be accessed. Note that a selection mechanism is inherent since there are multiple registers present in the register bank] **coupled to the register bank** [as shown in figure 2]; **and**

a first processor [the MPU, figure 2, 15] **coupled to the bus controller and the select register** [figure 2 shows that the MPU (figure 2, 15) is couple do the bus controller (the corresponding bus controller comprises the MPU bus interface unit (figure 2, 15a) and the NAND bus interface (figure 2, 19)) and the select register (figure 2, 22)].

As to claim 2, Sukegawa et al. teach that **the memory device controller of claim 1, further comprising an expression checker coupled between the first processor and the bus controller** [the corresponding expression check is the ECC unit (figure 2, 21) that checks the error correction code of the NAND EEPROM (column 18, lines 4-14)].

As to claim 3, Sukegawa et al. teach that **the memory device controller of claim 1, further comprising a transfer register** [the corresponding transfer register is the status register (figure 2, 177)] **coupled to the bus controller** [as shown in figure 2] **for receiving the third signal** [the third signal may be the status of the NAND EEPROM when the command is to inquire about the status of the NAND EEPROM] **therefrom during a first clock phase, and coupled to the register bank for**

transmitting the third signal thereto during a second clock phase [figures 18A~18G, 20A~20G, 22A~22G and 25A~25B show the timing sequence of the events according to the phases of clock].

As to claim 4, Sukegawa et al. teach that **the memory device controller of claim 1, further comprising a clock for sending clock signals to at least one of the first processor, the register bank, and the select register** [figures 18A~18G, 20A~20G, 22A~22G and 25A~25B show the timing sequence of the events according to the phases of clock].

As to claim 6, Sukegawa et al. teach that **the memory device controller of claim 1, further comprising a controller interface** [the buffer memory controller, figure 2, 18] **coupled to the first processor** [the MPU, figure 2, 15] **and couplable to at least one of a command user interface** [the external bus interface (figure 2, 17) to interface with an external command user (the CPU, figure 2, 1)] **of the memory device** [figure 2, 10] **and a second processor located externally of the memory device** [the CPU, figure 2, 1 is the second processor located externally].

As to claim 8, Sukegawa et al. teach that **the first signal comprises an address of the analog/memory core** [the corresponding first signal is the address signal (address conversion table, figure 2, 132)].

As to claim 9, Sukegawa et al. teach that **the bus controller comprises an arithmetic logic unit** [the ECC calculation unit (figure 2, 21; figure 16A, 21; figure 16B, 21)] **adapted to perform at least one arithmetic operation** [the ECC calculation

(column 16, lines 47-51)] **on at least one of the second signal and data received from the first processor** [column 18, lines 1-13].

As to claim 10, Sukegawa et al. teach that **the first processor** [the MPU, figure 2, 15] **comprises a storage device** [the ROM, figure 2, 16] **that contains one or more algorithms that include instructions for controlling operation of the memory device controller** [The microprocessor 15 executes firmware stored in the ROM 16 to control the operation of the entire semiconductor disk system 10 (column 15, lines 34-36)].

As to claim 11, Sukegawa et al. teach **a memory device controller comprising:**

an updateable register bank adapted to send a first signal to an analog/memory core of the memory device for controlling operation of the analog/memory core [refer to "As to claim 1"];

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank; a select register coupled to the register bank [refer to "As to claim 1"];

a first processor coupled to the bus controller and the select register [refer to "As to claim 1"];

an expression checker coupled between the first processor and the bus controller [refer to "As to claim 2"];

a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for

transmitting the third signal thereto during a second clock phase [refer to "As to claim 3"]; **and**

a controller interface coupled to the first processor and couplable to at least one of a command user interface [refer to "As to claim 6"] **of the memory device and a second processor located externally of the memory device** [refer to "As to claim 6"].

As to claim 12, refer to "As to claim 9" presented earlier in this Office Action.

As to claim 14, Sukegawa et al. teach **a memory device comprising**

an analog/memory core comprising an array of flash memory cells and supporting analog access circuitry [blocks of NAND EEPROM memory cells (figure 2, 11-1~11-16)];

a memory device controller comprising:

an updateable register bank adapted to send a first signal to the analog/memory core for controlling operation of the analog/memory core [refer to "As to claim 1"];

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank [refer to "As to claim 1"];

a select register coupled to the register bank [refer to "As to claim 1"]; **and**

a first processor coupled to the bus controller and the select register [refer to "As to claim 1"]; **and**

a command user interface coupled to the first controller and couplable to a second processor located externally of the memory device [refer to "As to claim 6"].

As to claim 15, refer to "As to claim 2" presented earlier in this Office Action.

As to claim 16, refer to "As to claim 9" presented earlier in this Office Action.

As to claim 18, Sukegawa et al. teach **a memory device comprising an analog/memory core comprising an array of flash memory cells and supporting analog access circuitry** [blocks of NAND EEPROM memory cells (figure 2, 11-1~11-16)];

a memory device controller comprising:

an updateable register bank adapted to send a first signal to the analog/memory core for controlling operation of the analog/memory core [refer to "As to claim 1"];

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank [refer to "As to claim 1"];

a select register coupled to the register bank [refer to "As to claim 1"]; **and**

a first processor coupled to the bus controller and the select register [refer to "As to claim 1"];

an expression checker coupled between the first processor and the bus controller [refer to "As to claim 2"];

a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for

transmitting the third signal thereto during a second clock phase [refer to "As to claim 3"]; **and**

a command user interface coupled to the first controller and couplable to a second processor located externally of the memory device [refer to "As to claim 6"].

As to claim 19, refer to "As to claim 18" presented earlier in this Office Action.

As to claim 20, refer to "As to claim 2" presented earlier in this Office Action.

As to claim 21, refer to "As to claim 9" presented earlier in this Office Action.

As to claim 23, refer to "As to claim 3" presented earlier in this Office Action.

As to claim 24, Sukegawa et al. teach **a method of operating a memory device controller** [figure 2, 12; figures 17-23 show the method of operations], **the method comprising**:

receiving first data [the corresponding first data is the ECC check start command, figure 19, step A39] **at a bus controller** [figure 19 shows that the ECC check start command is received by the NAND bus interface unit] **of the memory device controller** [figure 2, 12] **from a first register** [the command register, figure 2, 176] **of a register bank** [figure 2, 171 shows the register bank comprising registers 171~178] **of the memory device controller** [figure 2, 12];

sending second data [the corresponding second data is the ECC status data, figure 19, step B37] **from the bus controller** [figure 19 shows that the ECC status data is sent by the NAND bus interface unit] **to the first or a second register** [the status register, figure 2, 177] **of the register bank** [figure 2, 171 shows the register bank comprising registers 171~178] **for updating the register bank**; **and**

sending a control signal [the corresponding control signal is the ECC error signal, figure 19, step A41] **from a third register** [the error register, figure 2, 178] **of the register bank** [figure 2, 171 shows the register bank comprising registers 171~178] **to an analog/memory core** [NAND EEPROM, figure 2, 11-1~11-16] **of the memory device** [figure 2, 10] **for controlling operation of the analog/memory core** [verifying if ECC data from the memory is correct and if error correction is needed (column 18, lines 4-14)], **the analog/memory core comprising an array of flash memory cells and supporting analog access circuitry** [NAND EEPROM, figure 2, 11-1~11-16].

As to claim 25, Sukegawa et al. teach that **the method of claim 24, further comprising processing the first data** [the corresponding first data is the ECC check start command, figure 19, step A39] **at the bus controller** [figure 19 shows that the ECC check start command is received by the NAND bus interface unit] **to produce the second data** [the corresponding second data is the ECC status data, figure 19, step B37].

As to claim 26, Sukegawa et al. teach that **the method of claim 25, wherein processing the first data** [the corresponding first data is the ECC check start command, figure 19, step A39] **at the bus controller** [figure 19 shows that the ECC check start command is received by the NAND bus interface unit] **is in response to receiving a signal** [figure 19 shows that the NAND bus interface unit (19) receives a plurality of commands (A31~A37) leading to the ECC check start command (A39)] **from a processor** [the microprocessor, figure 19, 14] **of the memory device controller** [the MPU (figure 2, 18) is part of the controller (figure 2, 12)].

As to claim 27, Sukegawa et al. teach that **the method of claim 25, wherein processing the first data at the bus controller comprises processing the first data in combination with third data received at the bus controller from a processor of the memory device controller** [figure 19 shows that the NAND bus interface unit (19) receives a plurality of commands (A31~A37) leading to the ECC check start command (A39)] **from a processor** [the microprocessor, figure 19, 14].

As to claim 28, Sukegawa et al. teach **that the method of claim 24, wherein sending second data from the bus controller to the first or the second register comprises**:

sending the second data to a transfer register during a first clock phase [figures 20A~20G shows the timing sequence of the corresponding events illustrated in figure 19];

holding the second data at the transfer register until a second clock phase [figures 20A~20G shows the timing sequence of the corresponding events illustrated in figure 19]; **and**

sending the second data to the first or the second register during the second clock phase [figures 20A~20G shows the timing sequence of the corresponding events illustrated in figure 19].

As to claim 30, Sukegawa et al. teach **the method of claim 24, further comprising receiving an input signal at a third register of the register bank from the analog/memory core, the third signal indicative of operation of the analog/memory core** [the status registers, figure 2, 177; status managing means,

having a plurality of input ports for receiving the output ready/busy signals from the flash memories, for managing a status of each of the flash memories in accordance with a corresponding input ready/busy signal (column 3, lines 50-60)].

As to claim 31, Sukegawa et al. teach **the method of claim 24, further comprising receiving a control signal at a select register** [the address conversion table, figure 2, 132, contains the address information of an entity to be accessed. Note that a selection mechanism is inherent since there are multiple registers present in the register bank] **of the memory device controller from a processor** [the MPU (figure 2, 18) is part of the controller (figure 2, 12)] **of the memory device controller before receiving the first data at the bus controller for selecting the first register** [figure 19 shows that the NAND bus interface unit (19) receives a plurality of commands (A31~A37) leading to the ECC check start command (A39)].

Claim Rejections - 35 USC § 103

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa et al. (U.S. 5,603,001).

As to claim 5, Sukegawa et al. do not mention that **the clock comprises four clock phases.**

However, Sukegawa et al. illustrate in figures 18A~18G, 20A~20G, 22A~22G and 25A~25B the timing sequence of the events according to the phases of clock, which implies that a series of clocks are used to facilitate the operations. The exact number of clocks, be it three, four or five, may vary depending each operations and lacks patentable significance.

10. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Robinson et al., (US 5,544,356), "Block-Erasable Non-Volatile Semiconductor memory Which Tracks and Stores the Total Number of Write/Erase Cycles for Each block."
- Norman, (US 5,754,567), "Write Reduction in Flash Memory Systems through ECC Usage."
- Ideta, (US 6,038,635), "Microprocessor Containing Flash EEPROM Therein."
- Gelke et al., (US 6,735,661), "Integrated Circuit with Flash Memory including Dedicated Flash Bus and Flash Brideg."
- Zook, (US 5,668,976), "Error Correction Method and Apparatus for Disk Drive Emulator."
- Hasbun, (US 5,671,388), "Method and Apparatus for Performing Write Operations in Multi-Level Cell Storage Device."

Conclusion

11. Claims 1-28 and 30-31 are rejected as explained above.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

April 26, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
6/15/06